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# DATA SHEET

# BLF547
UHF push-pull power MOS transistor

Product specification

October 1992

Philips Semiconductors

PHILIPS

# UHF push-pull power MOS transistor BLF547

## FEATURES

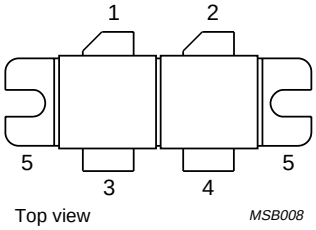
- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

## DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262A2 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

## PIN CONFIGURATION



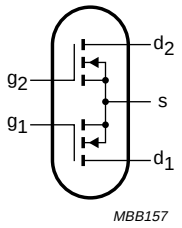




Fig.1 Simplified outline and symbol.

## CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

## PINNING - SOT262A2

| PIN | DESCRIPTION |
|---|---|
| 1 | drain 1 |
| 2 | drain 2 |
| 3 | gate 1 |
| 4 | gate 2 |
| 5 | source |

## WARNING

**Product and environmental safety - toxic materials**

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

## QUICK REFERENCE DATA

RF performance at $T_h$ = 25 °C in a push-pull common-source test circuit.

| MODE OF OPERATION | f (MHz) | $V_{DS}$ (V) | $P_L$ (W) | $G_P$ (dB) | $\eta_D$ (%) |
|---|---|---|---|---|---|
| CW, class-B | 500 | 28 | 100 | > 10 | > 50 |

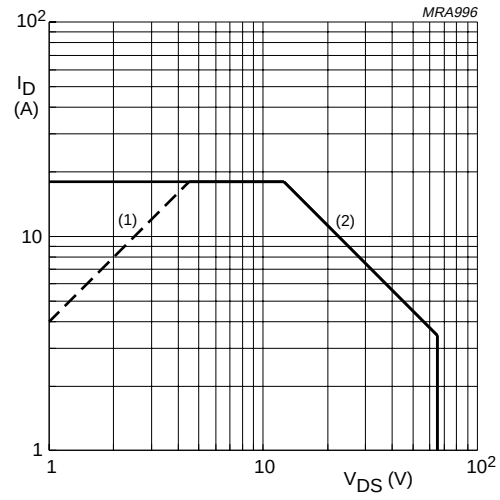
## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | | – | 65 | V |
| $\pm V_{GS}$ | gate-source voltage | | – | 20 | V |
| $I_D$ | DC drain current | | – | 9 | A |
| $P_{tot}$ | total power dissipation | up to $T_{mb}$ = 25 °C; total device; both sections equally loaded | – | 225 | W |
| $T_{stg}$ | storage temperature | | –65 | 150 | °C |
| $T_j$ | junction temperature | | – | 200 | °C |

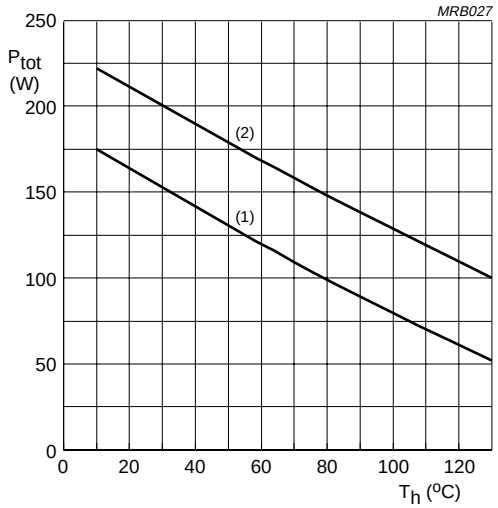
## THERMAL RESISTANCE

| SYMBOL | PARAMETER | CONDITIONS | THERMAL RESISTANCE |
|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | thermal resistance from junction to mounting base | $T_{mb}$ = 25 °C; $P_{tot}$ = 225 W total device; both sections equally loaded | max. 0.78 K/W |
| $R_{th\ mb\text{-}h}$ | thermal resistance from mounting base to heatsink | total device; both sections equally loaded | max. 0.15 K/W |




(1) Current in this area may be limited by $R_{DS(on)}$.
(2) $T_{mb}$ = 25 °C;
Total device; both sections equally loaded.

Fig.2 DC SOAR.



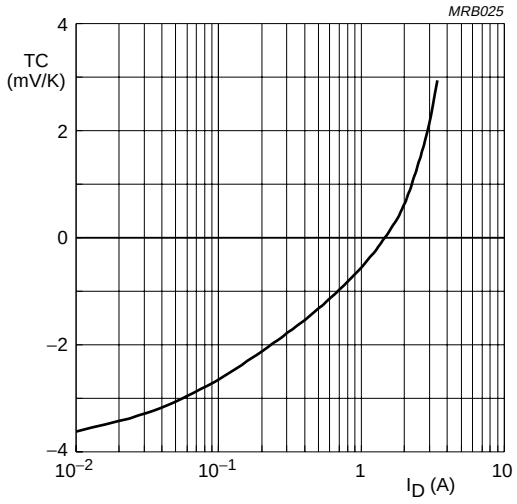

(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

**CHARACTERISTICS (per section)**

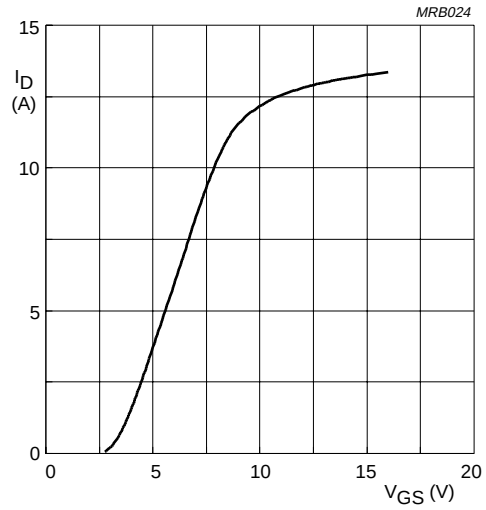
$T_j$ = 25 °C unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS}$ = 0; $I_D$ = 25 mA | 65 | – | – | V |
| $I_{DSS}$ | drain-source leakage current | $V_{GS}$ = 0; $V_{DS}$ = 28 V | – | – | 2.5 | mA |
| $I_{GSS}$ | gate-source leakage current | $\pm V_{GS}$ = 20 V; $V_{DS}$ = 0 | – | – | 1 | μA |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 100 mA; $V_{DS}$ = 10 V | 1 | – | 4 | V |
| $g_{fs}$ | forward transconductance | $I_D$ = 3 A; $V_{DS}$ = 10 V | 1.5 | 2.1 | – | S |
| $R_{DS(on)}$ | drain-source on-state resistance | $I_D$ = 3 A; $V_{GS}$ = 10 V | – | 0.4 | 0.5 | Ω |
| $I_{DSX}$ | on-state drain current | $V_{GS}$ = 15 V; $V_{DS}$ = 10 V | 10 | 13 | – | A |
| $C_{is}$ | input capacitance | $V_{GS}$ = 0; $V_{DS}$ = 28 V; f = 1 MHz | – | 77 | 85 | pF |
| $C_{os}$ | output capacitance | $V_{GS}$ = 0; $V_{DS}$ = 28 V; f = 1 MHz | – | 62 | 70 | pF |
| $C_{rs}$ | feedback capacitance | $V_{GS}$ = 0; $V_{DS}$ = 28 V; f = 1 MHz | – | 18 | 21 | pF |



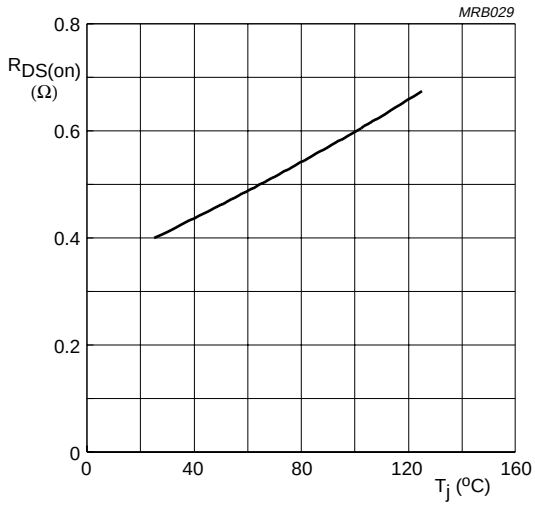

$V_{DS}$ = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



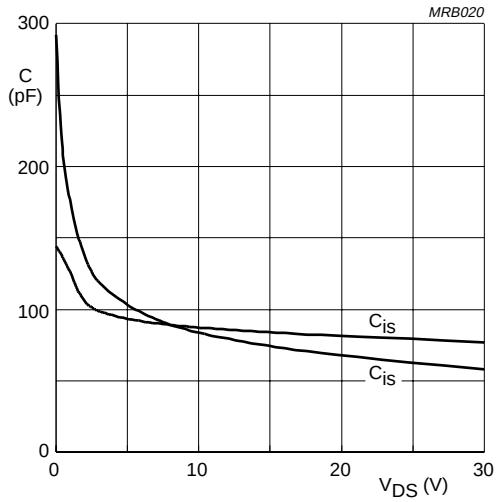

$V_{DS}$ = 10 V; $T_j$ = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



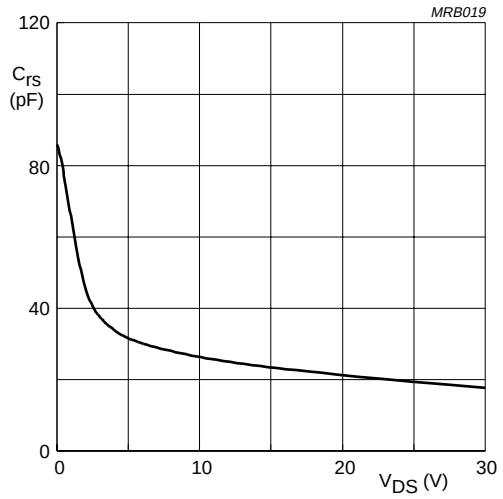

$I_D$ = 3 A; $V_{GS}$ = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.




$V_{GS}$ = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.




$V_{GS}$ = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

## APPLICATION INFORMATION FOR CLASS-B OPERATION

$T_h$ = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W, unless otherwise specified.

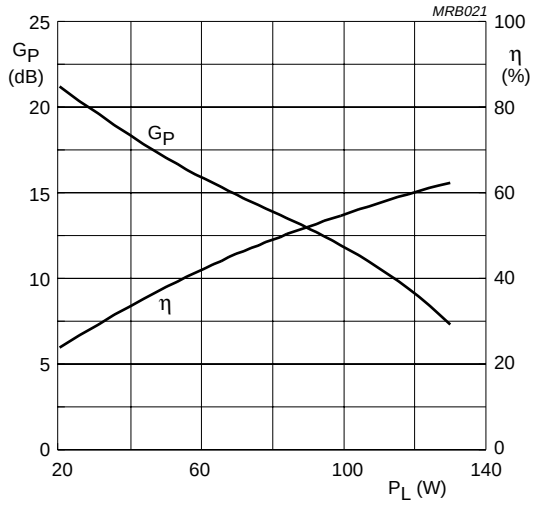
RF performance in a common source, push-pull, class-B test circuit.

| MODE OF OPERATION | f (MHz) | $V_{DS}$ (V) | $I_{DQ}$ (mA) | $P_L$ (W) | $G_P$ (dB) | $\eta_D$ (%) |
|---|---|---|---|---|---|---|
| CW, class-B | 500 | 28 | $2 \times 100$ | 100 | $> 10$ typ. 12 | $> 50$ typ. 55 |

### Ruggedness in class-B operation

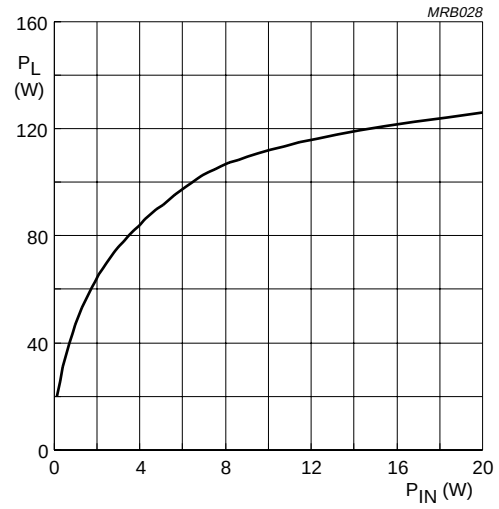
The BLF547 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

$V_{DS}$ = 28 V; f = 500 MHz at rated output power.



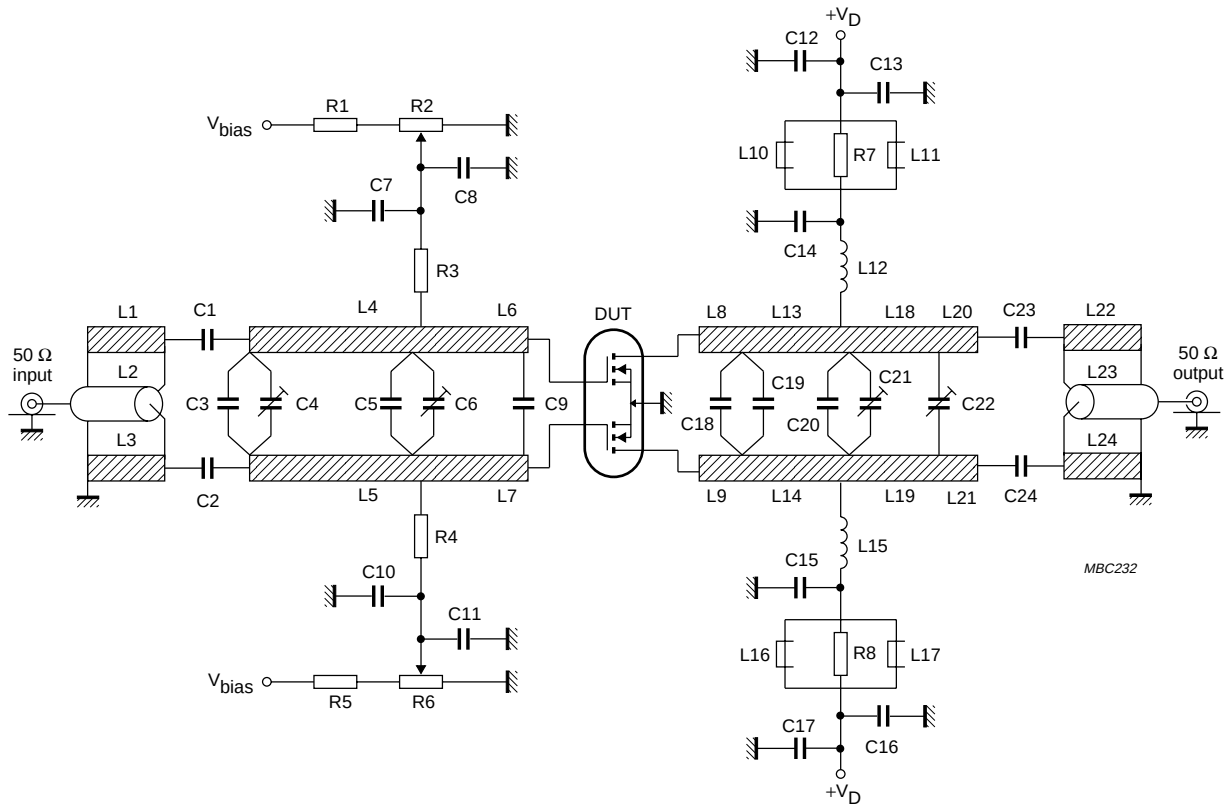

Class-B operation; $V_{DS}$ = 28 V; $I_{DQ} = 2 \times 100$ mA; f = 500 MHz; $Z_L = 1.5 + j1.8\ \Omega$ (per section).

Fig.9 Power gain and efficiency as functions of load power, typical values.




Class-B operation; $V_{DS}$ = 28 V; $I_{DQ} = 2 \times 100$ mA; f = 500 MHz; $Z_L = 1.5 + j1.8\ \Omega$ (per section).

Fig.10 Load power as a function of input power, typical values.




f = 500 MHz.

Fig.11 Test circuit for class-B operation.

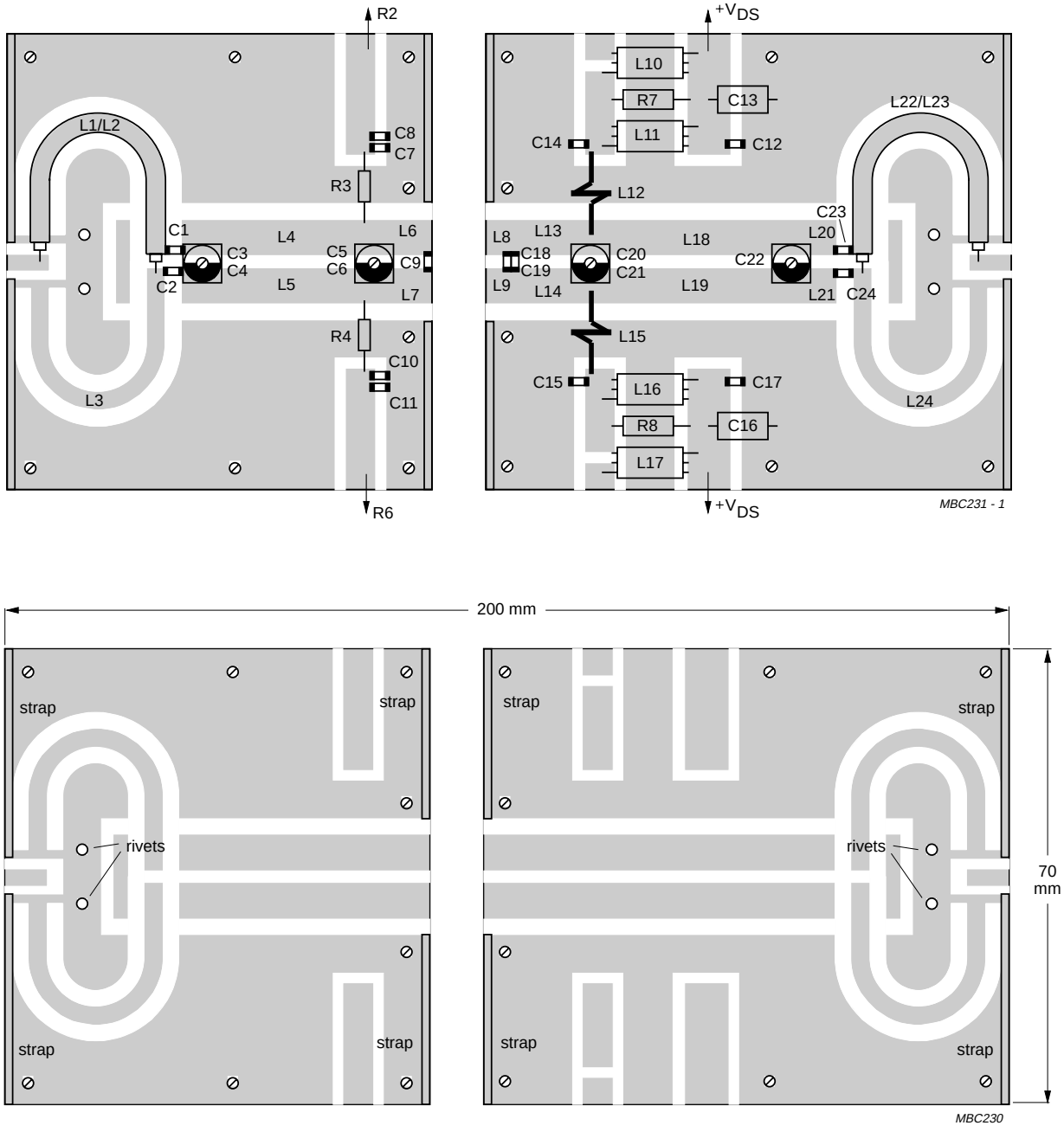
**List of components (see class-B test circuit)**

| COMPONENT | DESCRIPTION | VALUE | DIMENSIONS | CATALOGUE NO. |
|---|---|---|---|---|
| C1, C2 | multilayer ceramic chip capacitor (note 1) | 15 pF | | |
| C3 | multilayer ceramic chip capacitor (note 1) | 16 pF | | |
| C4 | film dielectric trimmer | 2 to 9 pF | | 2222 809 09005 |
| C5 | multilayer ceramic chip capacitor (note 2) | 15 pF | | |
| C6, C21, C22 | film dielectric trimmer | 2 to 18 pF | | 2222 809 09006 |
| C7, C10, C14, C15 | multilayer ceramic chip capacitor (note 1) | 390 pF | | |
| C8, C11, C12, C17 | multilayer ceramic chip capacitor | 100 nF | | 2222 852 47104 |
| C9 | multilayer ceramic chip capacitor (note 3) | $2 \times 68$ pF in series | | |

| COMPONENT | DESCRIPTION | VALUE | DIMENSIONS | CATALOGUE NO. |
|---|---|---|---|---|
| C13, C16 | electrolytic capacitor | 10 μF, 63 V | | 2222 030 28109 |
| C18 | multilayer ceramic chip capacitor (note 2) | 10 pF | | |
| C19 | multilayer ceramic chip capacitor (note 2) | 27 pF | | |
| C20 | multilayer ceramic chip capacitor (note 2) | 8.2 pF | | |
| C23, C24 | multilayer ceramic chip capacitor (note 1) | 30 pF | | |
| L1, L3, L22, L24 | stripline (note 4) | 34.5 Ω | length 66.5 mm<br>width 4 mm | |
| L2, L23 | semi-rigid cable | 50 Ω | length 66.5 mm<br>width 3.6 mm | |
| L4, L5 | stripline (note 4) | 22.3 Ω | length 35 mm<br>width 7 mm | |
| L6, L7 | stripline (note 4) | 22.3 Ω | length 10 mm<br>width 7 mm | |
| L8, L9 | stripline (note 4) | 22.3 Ω | length 5.5 mm<br>width 7 mm | |
| L10, L11, L16, L17 | grade 3B Ferroxcube RF choke | | | 4312 020 36640 |
| L12, L15 | 1 turn enamelled 1.5 mm copper wire | 17 nH | length 5 mm<br>int. dia. 9 mm<br>leads 2 × 5 mm | |
| L13, L14 | stripline (note 4) | 22.3 Ω | length 15 mm<br>width 7 mm | |
| L18, L19 | stripline (note 4) | 22.3 Ω | length 36 mm<br>width 7 mm | |
| L20, L21 | stripline (note 4) | 22.3 Ω | length 8.5 mm<br>width 7 mm | |
| R1, R5 | 0.4 W metal film resistor | 24.7 kΩ | | 2322 151 72473 |
| R2, R6 | 10 turn potentiometer | 5 kΩ | | |
| R3, R4 | 0.4 W metal film resistor | 10.5 kΩ | | 2322 151 71053 |
| R7, R8 | 1 W metal film resistor | 10 Ω | | 2322 151 71009 |

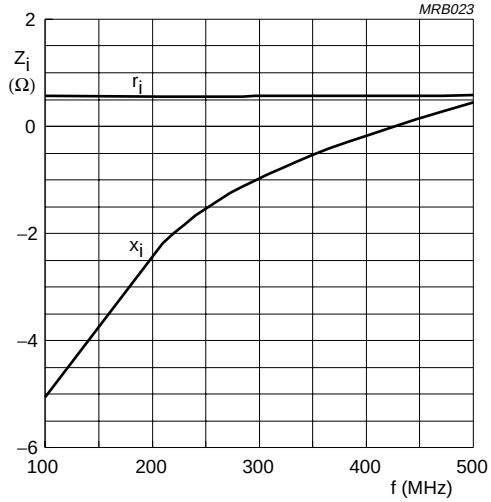
**Notes**

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
4. The striplines are on a double copper-clad printed circuit board, with PTFE fiber-glass dielectric ($\varepsilon_r$ = 2.2), thickness 0.79 mm.



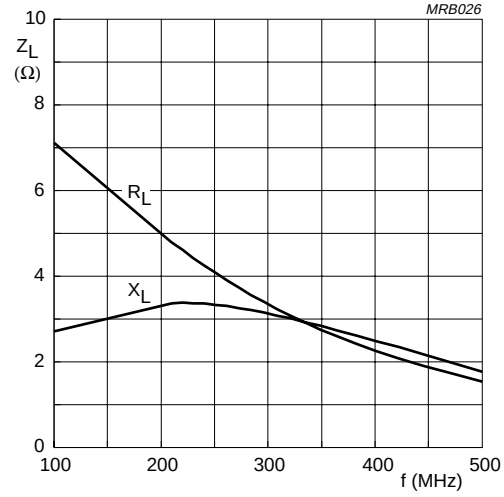

The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized to serve as a ground plane. Connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.




Class-B operation; $V_{DS}$ = 28 V; $I_{DQ}$ = 100 mA (per section); $P_L$ = 100 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.




Class-B operation; $V_{DS}$ = 28 V; $I_{DQ}$ = 100 mA (per section); $P_L$ = 100 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

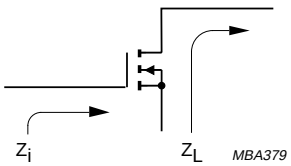
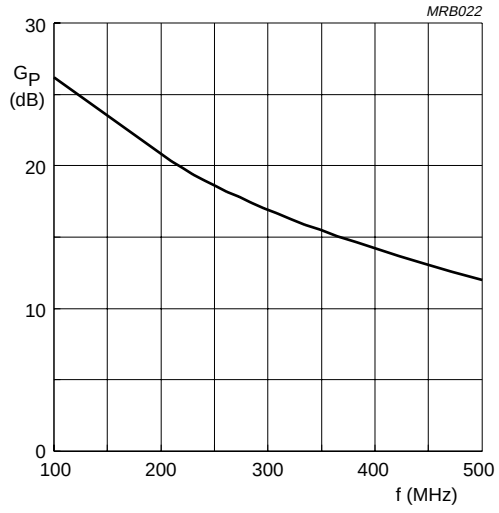



Fig.15 Definition of MOS impedance.

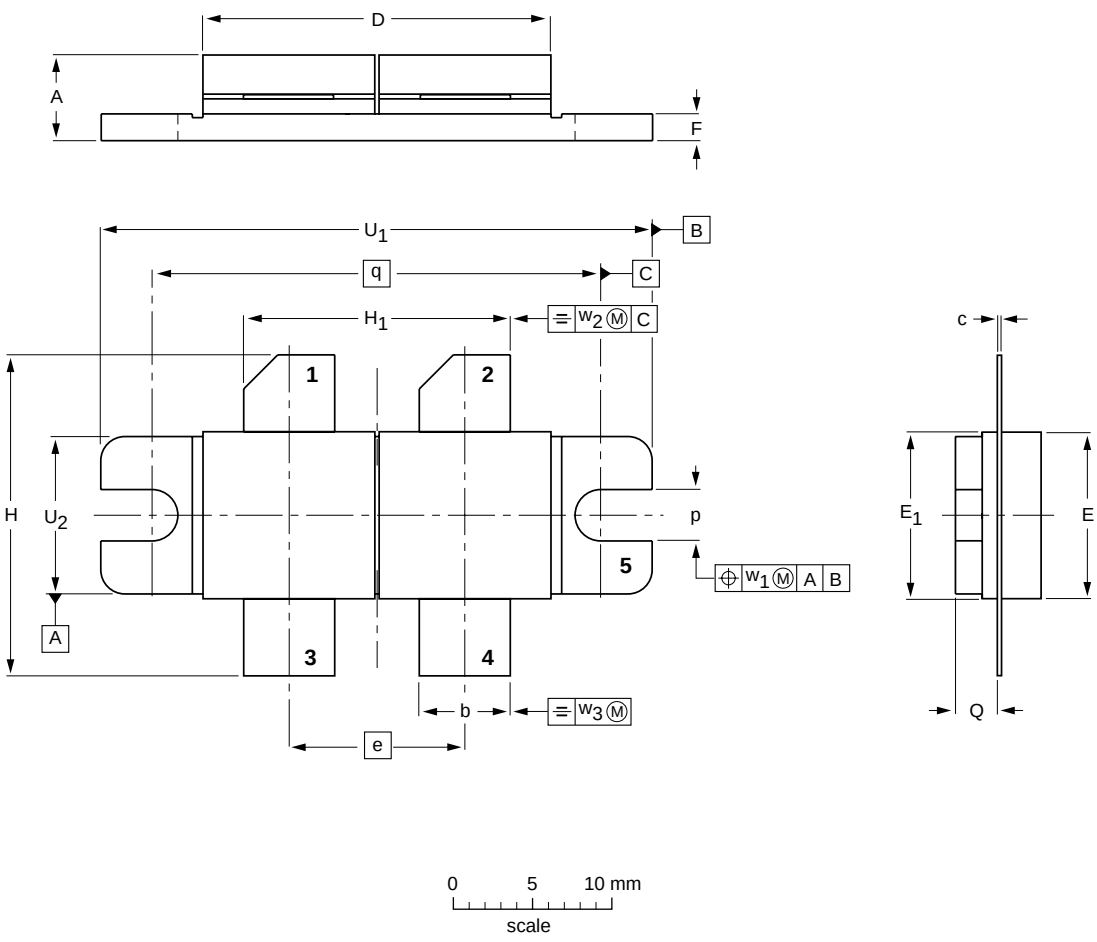



Class-B operation; $V_{DS}$ = 28 V; $I_{DQ}$ = 100 mA (per section); $P_L$ = 100 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

## PACKAGE OUTLINE

**Flanged double-ended ceramic package; 2 mounting holes; 4 leads** **SOT262A2**




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

| UNIT | A | b | c | D | e | E | $E_1$ | F | H | $H_1$ | p | Q | q | $U_1$ | $U_2$ | $w_1$ | $w_2$ | $w_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.39<br>4.62 | 5.85<br>5.58 | 0.16<br>0.10 | 21.98<br>21.71 | 11.05 | 10.27<br>10.05 | 10.29<br>10.03 | 1.78<br>1.52 | 20.58<br>20.06 | 17.02<br>16.51 | 3.28<br>3.02 | 2,47<br>2.20 | 27.94 | 34.17<br>33.90 | 9.91<br>9.65 | 0.51 | 1.02 | 0.25 |
| inches | 0.212<br>0.182 | 0.230<br>0.220 | 0.006<br>0.004 | 0.865<br>0.855 | 0.435 | 0.404<br>0.395 | 0.405<br>0.396 | 0.070<br>0.060 | 0.81<br>0.79 | 0.67<br>0.65 | 0.129<br>0.119 | 0.097<br>0.087 | 1.100 | 1.345<br>1.335 | 0.390<br>0.380 | 0.02 | 0.04 | 0.01 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT262A2 | | | | | | 97-06-28 |

**DEFINITIONS**

| **Data Sheet Status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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